SPECIFICATION

At page 6, please amend paragraph [0030] as follows:

[0030] As shown in FIG. 1, the EMI cancellation system according to the embodiment of the present invention comprises a control signal generation unit (100), a voltage control unit (200), and an oscillator (300). The control signal generation unit (100) receives a clock signal (CLK) initially outputted from the oscillator (300) so as to generate n control signals ~~(S1-Sn)~~ (S_1-S_n). The voltage control unit (200) outputs voltage ~~(Vhigh)~~(V_{high}) of n levels according to the control signal ~~(S1-Sn)~~ (S_1-S_n).

At page 6, please amend paragraph [0032] as follows:

[0032] As shown in FIG. 2 and FIG. 3, the control signal generation unit (100) includes a counter (110), a flip-flop (120), and a multiplexer (130). The counter (110) includes n flip-flops ~~(FF1-FFn)~~ (FF_1-FF_n) such that an output of the flip-flop ~~(FFn)~~ (FF_n) becomes an input of the flip-flop (120). Each of the flip-flops ~~(FF1-FFn)~~ (FF_1-FF_n) outputs a pair of a normal and a reverse signal ~~(Q1-Qn, QB1-QBn)~~ (Q_1-Q_n, QB_1-QB_n) and is triggered at a rising edge of a clock signal (CLK) and an output signal ~~(Q1-Qn-1)~~ (Q_1-Q_{n-1}) of the previous flip-flop ~~(FF1-FFn-1)~~ (FF_1-FF_{n-1}) so as to reverse the state of the output signal ~~(Q1-Qn, QB1-QBn)~~ (Q_1-Q_n, QB_1-QB_n). That is, the output ~~(Q1-Qn, QB1-QBn)~~ (Q_1-Q_n, QB_1-QB_n) of each flip-flop ~~(FF1-FFn)~~ (FF_1-FF_n) reverses at every cycle of the signals (CLC and ~~Q1-Qn-1~~ Q_1-Q_{n-1}) inputted to the flip-flop ~~(FF1-FFn)~~ (FF_1-FF_n). Identically, the flip-flop (120) outputs a pair of a normal and a reverse state signal (Q and QB) and reverses the state of output signals (Q, QB) by being triggered at the rising edge of the output signal ~~(Qn)~~ (Q_n) of the final flip-flop ~~(FFn)~~ (FF_n) of the counter (110).

At page 7, please amend paragraph [0033] as follows:

[0033] The multiplexer (130) includes 2n transmission gates ~~(TG1-TGn, TGB1-TGBn)~~ (TG_1-TG_n, TGB_1-TGB_n). The transmission gate ~~(TG1-TGn)~~ (TG_1-TG_n) receives an output signal ~~(Q1-Qn)~~ (Q_1-Q_n) of the flip-flop ~~(FF1-FFn)~~ (FF_1-FF_n), and the transmission gate

~~(TGB1-TGBn)~~ (TGB_1-TGB_n) receives an output signal ~~(QB1-QBn)~~ (QB_1-QB_n) of the flip-flop ~~(FF1-FFn)~~ (FF_1-FF_n). The two transmission gates ~~(TG1-TGn, TGB1-TGBn)~~ (TG_1-TG_n, TGB_1-TGB_n) transfer the output signals ~~(Q1-Qn or QB1-QBn)~~ (Q_1-Q_n or QB_1-QB_n) of each flip-flop ~~(FF1-FFn)~~ (FF_1-FF_n) according to the states of the output signals (Q, QB).

At page 7, please amend paragraph [0034] as follows:

[0034] An operation of the control signal generation unit (100) according to the embodiment of the present invention will be described in more detail hereinafter with reference to FIG. 4. In FIG. 4, it is assumed that the counter (110) has 4 flip-flops ~~(FF1-FF4)~~ (FF_1-FF_4) so as to generate 4 control signals ~~(S1-S4)~~ (S_1-S_4) for convenience of explanation.

At page 7, please amend paragraph [0036] as follows:

[0036] As shown in FIG. 4, the output signal ~~(Q1)~~ (Q_1) of the flip-flop ~~(FF1)~~ (FF_1) is triggered to rise at the rising edge of the clock signal (not shown) and to fall at the next rising edge of the clock signal (CLK). Identically, the output signal ~~(Q2)~~ (Q_2) of the flip-flop ~~(FF2)~~ (FF_2) is triggered to rise and fall at the rising edges of the output signal ~~(Q1)~~ (Q_1) of the flip-flop ~~(FF1)~~ (FF_1). In this manner, the output signal (Q) of the flip-flop (120) is triggered to rise and fall at the rising edges of the output signal ~~(Q4)~~ (Q_4) of the final flip-flop ~~(FF4)~~ (FF_4). The output signal (QB) of the flip-flop (120) is a reverse signal of the output signal (Q).

At page 7, please amend paragraph [0037] as follows:

[0037] In FIG. 3, the output signals (Q, QB) of the flip-flop (120) are inputted to the respective transmission gates ~~(TG1-TG4, TBG1-TBG4)~~ (TG_1-TG_4, TBG_1-TBG_4). Here, when the output signal (Q) of the flip-flop (120) is high and the output signal (QB) of the flip-flop (120) is low, the transmission gate ~~(TG1-TG4)~~ (TG_1-TG_4) passes the output signal ~~(QB1-QB4)~~ (QB_1-QB_4) as a control signal ~~(S1-S4)~~ (S_1-S_4).

At page 8, please amend paragraph [0038] as follows:

[0038] Accordingly, as shown in FIG. 4, when the output signal (Q) of the flip-flop (120) is high, the output signal ~~(Q1-Q4)~~ (Q_1-Q_4) is outputted as the control signal ~~(S1-S4)~~ (S_1-S_4) for the control signal generation unit (100), and when the output signal (Q) of the flip-flop (120) is low, the reverse signal ~~(QB1-QB4)~~ (QB_1-QB_4) of the output signal ~~(Q1-Q4)~~ (Q_1-Q_4) is outputted as the control signal ~~(S1-S4)~~ (S_1-S_4). That is, the counter 110 alternately outputs the output signals ~~(Q1-Qn)~~ (Q_1-Q_n) and the inverted output signals ~~(QB1-QBn)~~ (QB_1-QB_n) as control signals ~~(S1-Sn)~~ (S_1-S_n) according to the period of counting n bits.

At page 8, please amend paragraph [0039] as follows:

[0039] A method for generating clock signals having various frequencies according to the control signals ~~(S1-Sn)~~ (S_1-S_n) generated in this manner will be described with reference to FIG. 5 to FIG. 8.

At page 8, please amend paragraph [0041] as follows:

[0041] As shown in FIG. 5, the voltage control unit (200) includes ~~24~~ 16 ~~registers~~ resistors (R) (typically ~~2n~~ 2^n), 15 (=8+4+2+1) ~~(=23+22+2+1)~~ NMOS transistors ~~(N1-N15)~~ (N_1-N_{15}), and 15 (=8+4+2+1) ~~(=23+22+2+1)~~ PMOS transistors ~~(P1-P15)~~ (P_1-P_{15}). The ~~registers~~ resistors (R) are coupled in series between a power supply voltage (Vdd) and a ground voltage, and the NMOS transistors ~~(N1-N8)~~ (N_1-N_8) and the PMOS transistors ~~(P1-P8)~~ (P_1-P_8) are alternately coupled to the terminals of the ~~registers~~ resistors (R). The NMOS transistors ~~(N1-N8)~~ (N_1-N_8) and the PMOS transistors ~~(P1-P8)~~ (P_1-P_8) are coupled in parallel to the resistors R, and NMOS transistors ~~(N13, N14)~~ (N_{13}, N_{14}) and PMOS transistors ~~(P13, P14)~~ (P_{13}, P_{14}) are alternately coupled to nodes of the NMOS transistors ~~(N1-N8)~~ (N_1-N_8) and the PMOS transistors ~~(P1-P8)~~ (P_1-P_8). Also, NMOS and PMOS transistors ~~(N15, P15)~~ (N_{15}, P_{15}) are coupled to the nodes of the NMOS and PMOS transistors ~~(N13, P13, N 14, P14)~~ (N_{13}, P_{13}, N_{14}, P_{14}), respectively.

At page 9, please amend paragraph [0042] as follows:

[0042] For example, the transistors ~~(N1, N9, N13, N15)~~ (N_1, N_9, N_{13}, N_{15}) output the power supply voltage (Vdd) when the control signal ~~(S1-S4)~~ (S_1-S_4) is "1111", and output 15/16 of the power supply voltage when the transistors ~~(N1, N9, N13, N15)~~ (N_1, N_9, N_{13}, N_{15}) are "0111." In this manner, the transistors ~~(P8, P12, P14, P15)~~ (P_8, P_{12}, P_{14}, P_{15}) output 1/16 of the power supply voltage (Vdd).

At page 9, please amend paragraph [0043] as follows:

[0043] Accordingly, the voltage control unit (200) can output the voltages ~~(V1-Vn)~~ (V_1-V_n) of 2n levels that increase or decrease stepwise, as shown in FIG. 6. Of course, the voltage control unit (200) can be implemented in another structure so as to output the control signals ~~(S1-Sn)~~ (S_1-S_n) that increase and decrease stepwise.

At page 9, please amend paragraph [0044] as follows:

[0044] The voltages ~~(V1-Vn)~~ (V_1-V_n) outputted from the voltage control unit (200) are inputted to the oscillator (300) of FIG. 7 as a high voltage level ~~(Vhigh)~~ (V_{high}). When an inputted sawtooth signal is charged to reach each stepwise voltage ~~(V1-Vn)~~ (V_1-V_n), the oscillator (300) generates and outputs clock signals ~~(CLK1-CLKn)~~ (CLK_1-CLK_n). As shown in FIG. 8, the frequency of the clock signal ~~(CLK1-CLKn)~~ (CLK_1-CLK_n) decreases as the level of the stepwise voltage ~~(V1-Vn)~~ (V_1-V_n) increases. That is, the oscillator (300) generates the clock signal ~~(CLK1-CLKn)~~ (CLK_1-CLK_n) having a pulse width proportional to the difference between the high voltage level ~~(Vhigh)~~ (V_{high}) and lower voltage level ~~(Vlow)~~ (V_{low}). In this way the frequency of the clock signal ~~(CLK1-CLKn)~~ (CLK_1-CLK_n) can be adjusted in a predetermined range.